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Serial No.: 09/902,429

Case No: F0588

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE
THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Qi Xiang et al.

Serial No.: 09/902,429

Filing Date: July 10, 2001

For: SILICON ON INSULATOR FIELD EFFECT TRANSISTOR WITH HETEROJUNCTION GATE

Examiner: Laura M. Shillinger

Art Unit 2813

APPELLANTS' BRIEF

Box AF
Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

This is an appeal from the decision mailed on September 25, 2002, finally rejecting claims 1-14 and 22-27 in the above-identified application.

I. Real Party in Interest

The real party in interest is the assignee, Advanced Micro Devices, Inc.

II. Related Appeals and Interferences

There are presently no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of the Claims

Claims 1-27 are pending in the application. Claims 15-20 have been withdrawn from consideration. Claims 1-14 and 21-27 have been finally rejected.

The rejections of claims 1-14 and 22-27 are the subject of this appeal. Attached is Appendix A containing a copy of appealed claims 1-14 and 22-27.

IV. Status of Amendments

Applicants amended the claims most recently in their response to the Office Action mailed on March 19, 2002. All amendments to the claims have been entered.

V. Summary of the Invention

The present invention relates to the design of field effect transistors (FETs) formed on a silicon on insulator (SOI) wafer. A traditional field effect transistor has a source region, a drain region, and a channel region (of opposite semiconductor conductivity) separating the source region from the drain region. Above the channel region, and separated from the channel region by an insulating film, is a gate electrode. The insulating film enables capacitive coupling between the gate electrode and the channel region but prevents diffusion of charge between the gate electrode and the channel region. Control of the potential of the channel region affects the flow of current between the source region and the drain region.

The FET of applicants' invention has a source region, drain region, and channel region all of the same semiconductor conductivity (P6, L17-19) and does not have an insulating film between the gate electrode and the FET channel region (See Figure 1). Instead, the FET of applicant's invention comprises a silicon carbide gate electrode that is deposited on the surface of the channel region (P10, L24-25) and forms a semiconductor heterojunction with the channel region (P7, L19-20). The semiconductor

heterojunction (as opposed to an insulating film) limits diffusion of charge between the channel region and the gate electrode and enables capacitive coupling between the gate electrode and the channel region thereby controlling depletion within the channel region (P7, L21-24).

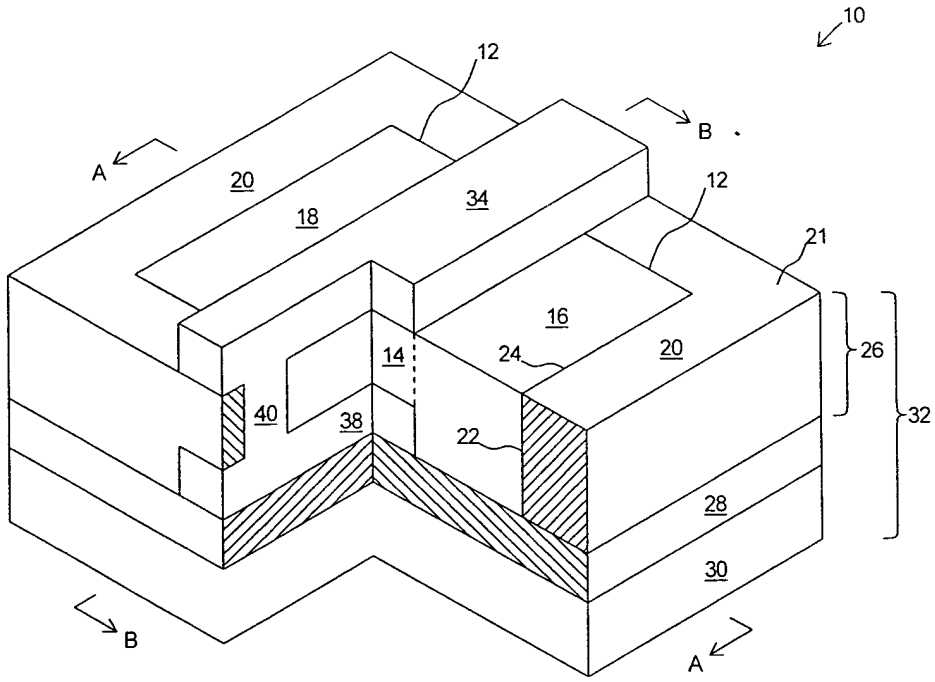

Figure 1

Fig. 1 (Applicants' Invention)

Figure 1 of the present application, shown above for convenience, illustrates the structure of the FET 10 of the applicant's invention.

The FET 10 is positioned within a thin silicon device layer 26 of an SOI wafer 32 (P6, L10-11). The SOI wafer includes an insulating layer 28 beneath the silicon device layer 26 and a silicon substrate 30 beneath the insulating layer 28 such that the insulating layer isolates silicon structures, such as the FET 10, from the silicon substrate 30 (P6, 11-14).

The FET 10 includes an active region 12 which is isolated from other structures by an insulating trench 20 extending from the surface 21 of the silicon device layer 32 down to the insulating layer 28 (P6, L20-21). The insulating trench 20 has side walls 22 which define the perimeter 24 of the active region 12 and function to isolate the active region 12 from other structures formed in the silicon device layer 26 (P6, L22-24).

The active region 12 comprises a central channel region 14, a source region 16, and a drain region 18 (P6, L15-16). The channel region 14 is lightly doped N-conductivity silicon and each of the source region 16 and the drain region 18 are each heavily doped N-conductivity silicon (P6, L16-19).

A silicon carbide gate 34 is positioned above the channel region 14. The silicon carbide gate 34 comprises silicon carbide implanted with a P-type impurity such as Boron (P6, 25-29). The silicon carbide gate 34 forms a semiconductor heterojunction with the channel region 14 (P7, L18-20).

Similarly, a silicon carbide backgate 38 is positioned below the channel region 14. The silicon carbide backgate also comprises silicon carbide implanted with a P-type impurity such as Boron (P6, L25-29). The silicon carbide backgate 38 forms a semiconductor heterojunction within a lower portion of the channel region 14 (P7, L18-20). A conductive via 40 is positioned within the insulating trench 20 and electrically couples the silicon carbide gate 34 to the silicon carbide backgate 38 (P6, L29-31).

It should be appreciated that carbon, having an energy gap greater than silicon, tends to increase minority carriers (e.g. free electrons) within the P-type silicon carbide gate 34 and the P-type silicon carbide backgate 38. As such, junction capacitance at the semiconductor junctions formed between the channel region 14 and each of the silicon carbide gate 34 and the silicon carbide backgate 38 is increased. The increased junction capacitance tends to increase the thickness of the depletion regions within the central channel region 14 without increasing the charge that diffuses from the channel

region 14 into the silicon carbide gate 34 and the silicon carbide backgate 38 (P7, L16-24).

In operation, the FET 10 is normally "off" when no current will flow from the source region 16 to the drain region 18. The "off" state is achieved when the potential of both the silicon carbide gate 34 and the silicon carbide backgate 38 are at ground potential. At ground potential, the depletion region on the upper portion of the central channel region 14 (controlled by potential applied to the silicon carbide gate 34) extends towards the depletion region on the lower portion of the central channel region 14 (controlled by potential applied to the silicon carbide backgate 38) and the two depletion regions "pinch-off" current flow between the source region 16 and the drain region 18 (P6, L32 through P7, L6).

When the potential of both the silicon carbide gate 34 is raised above a threshold potential, the semiconductor junction between the silicon carbide gate 34 and the channel region 14 enables carriers to accumulate within the depletion regions without diffusing into the silicon carbide gate 34 or the silicon carbide backgate 38. The accumulated carriers enable current flow from the source region 16 to the drain region 18 (P7 L7-15)

VI. Issues

The issues presented for appeal are:

A. *Whether claims 1-4, 8-11, and 22-27 are properly rejected under 35 USC §102(e) as being anticipated by Kumar et al.*

B. *Whether claims 5-7 and 12-14 are properly rejected under 35 USC §103(a) based on Kumar et al. in view of Yamazaki et al.*

VII. Grouping of the Claims

Claims 1, 8, 22, and 25 ("Group 1") stand or fall together as a group directed to a field effect transistor having a gate adjacent to a channel region and forming a junction

with the channel region. The gate comprising a first semiconductor (that is the same conductivity as the channel region) and being doped with a second impurity element to increase minority carriers.

Claims 2-7, 9-14, 23-24, and 26-27 ("Group 2") stand or fall together as a group directed to a field effect transistor having a gate adjacent to a channel region and forming a junction with the channel region, having a back gate adjacent to the channel region, forming a junction with the channel region, and on an opposing side of the channel region from the gate. The gate and the back gate both comprising a first semiconductor (that is the same conductivity as the channel region) and being doped with a second impurity element to increase minority carriers.

VIII. Argument

A. The Field Effect Transistor Recited in Claims 1-4, 8-11, and 22-27 is not taught or suggested by Kumar et al.

Group 1

Both independent claims 1 and 8 define a transistor structure that comprises a central channel region consisting of a first semiconductor lightly doped with a first impurity element to increase first conductivity free carriers. A source region and a drain region are positioned on opposing sides of the central channel region and both the source region and the drain region consist of the first semiconductor heavily doped with the first impurity element. A gate is positioned adjacent to the channel region and forms a junction with the channel region. The gate comprises the first semiconductor and a second semiconductor with an energy gap greater than the first semiconductor. The gate is also doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

Kumar et al. does not teach or suggest such a device. *Kumar et al.* teaches a

memory cell for charge storage. The *Kumar et al.* device includes a gate that is separated from a channel region by an oxide film. Because the device of *Kumar et al.* includes an oxide film separating a channel region from a gate, *Kumar et al.* does not teach a gate that is adjacent to the channel region and forming a junction with the channel region.

Claims 22 and 25 each depend from claims 1 or 8 and can be distinguished over *Kumar et al.* for at least the same reasons. Further, the additional features recited in such claims further serve to distinguish such claims over *Kumar et. al.* and the other art of record.

In summary, neither *Kumar et al.* nor the other art of record, alone, or in combination, discloses the structure claimed by the applicant in the independent claims (1 and 8) of the present application. And, by virtue of all other claims depending from one of claims 1 and 8, neither *Kumar et al.* nor the other art of record discloses the structure of such other claims. As a result, reversal of the rejection with respect to Group 1 claims is respectfully requested.

Group 2

Claims 2 and 9 each define the transistor structure of claims 1 and 8 respectively and further include a backgate adjacent to the channel region, forming a junction with the channel region, and on an opposing side of the channel region. The backgate also comprises the first semiconductor and a second semiconductor with an energy gap greater than the first semiconductor and is also doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

Claims 2 and 9 can each be distinguished over *Kumar et al.* for the same reasons as claim 1 and 8. Further, to the extent that *Kumar et al.* discloses a backgate, the backgate of *Kumar et al.* is separated from the channel region by an oxide film. *Kumar et al.* does not teach or suggest a backgate that is adjacent to the channel

region and forming a junction with the channel region.

Claims 3-4, 10-11, and 23-24 and 26-27 each depend from claims 2 or 9 and can be distinguished over *Kumar et al.* for at least the same reasons. Further, the additional features recited in such claims further serve to distinguish such claims over *Kumar et. al.* and the other art of record.

Neither *Kumar et al.* nor the other art of record, alone, or in combination, discloses the structure of claims 2 and 9. And, by virtue of claims 3-4, 10-11, 23-24, and 26-27 depending from one of claims 2 and 9, neither *Kumar et al.* nor the other art of record discloses the structure of such other claims. As a result, reversal of the rejection with respect to Group 2 claims is respectfully requested.

B. A. The Field Effect Transistor Recited in Claims 5-7 and 12-14 is not taught or suggested by Kumar et al. in view of Yamazaki et al.

Group 2

Claims 5 and 12 each depend from claims 4 and 11 respectively and further define the first conductivity free carriers as electrons and the second conductivity free carriers as holds.

In more detail, each of claims 5 and 12 define a transistor structure that comprises a central channel region consisting of silicon lightly doped with a first impurity element to increase electrons. A source region and a drain region are positioned on opposing sides of the central channel region and both the source region and the drain region consist of silicon heavily doped with the first impurity element.

A gate is positioned adjacent to the channel region and forms a junction with the channel region. The gate comprises silicon and carbon with an energy gap greater than silicon. The gate is also doped with a second impurity element to increase holes.

A backgate is positioned adjacent to the channel region, forms a junction with the channel region, and is on an opposing side of the channel region than the gate. The backgate also comprises silicon and carbon with an energy gap greater than silicon and is also doped with a second impurity element to increase holes.

The examiner asserts that *Kumar et al.* teaches all of the above described elements except for the first conductivity free carriers being electrons and the second conductivity free carriers being holes. The examiner admits that *Kumar et al.* fails to each such. The Examiner relies on *Yamazaki et al.* teaching that doping with Arsenic forms an N-type region wherein the carriers are electrons and that doping with Boron forms a P-type region whereby the carriers are holes.

As discussed with respect to the rejection under 35 USC §102, neither *Kumar et al.* nor any of the other art of record, alone, or in combination, discloses a transistor with i) a gate that is adjacent to the channel region and forms a junction with the channel region; and ii) a backgate that is adjacent to the channel region and forms a junction with the channel region.

Accordingly, neither the primary reference to *Kumar et al.* nor the secondary references to *Yamazaki et al.* (alone or in combination) teaches or suggest the field effect transistor of claims 5 and 12.

Claims 6-7 and 13-14 each depend from claims 5 or 12 and can be distinguished over a combination of both *Kumar et al.* and *Yamazaki et al.* for at least the same reasons. Further, the additional features recited in such claims further serve to distinguish such claims over the combination of *Kumar et. al.*, *Yamazaki et al.* and the other art of record.

As a result, reversal of the rejection is respectfully requested.

IX. Conclusion

For the reasons given above, appellants respectfully request that the rejections of claims 1-14 and 22-27 on appeal be reversed and that such claims be allowed.

Should a petition for an extension of time be necessary for the timely filing of Appellants' Brief (or if such a petition has been made and an additional extension is necessary), petition is hereby made and the Commissioner is authorized to charge any fees (including additional claim fees) to Deposit Account No. 18-0988.

Respectfully submitted,

RENNER, OTTO, BOISSELLE & SKLAR, L.L.P.

Mark D. Saralino
Reg. No. 34,243

DATE: March 13, 2003

The Keith Building
1621 Euclid Avenue
Nineteenth Floor
Cleveland, Ohio 44115
(216) 621-1113
C:\GEN\Yama\yamap539appbr.wpd

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March 13, 2003
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Appendix

1. A transistor structure comprising:

a) a central channel region consisting of a first semiconductor lightly doped with a first impurity element to increase first conductivity free carriers;

b) a source region and a drain region on opposing sides of the central channel region, both source region and the drain region consisting of the first semiconductor heavily doped with the first impurity element;

c) a gate adjacent the channel region and forming a junction with the channel region, the gate comprising the first semiconductor and a second semiconductor with an energy gap greater than the first semiconductor and being doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

2. The transistor structure of claim 1, further including a backgate adjacent the channel region, and on an opposing side of the channel region from the gate, and forming a junction with the channel region, the backgate comprising the first semiconductor and a second semiconductor with an energy gap greater than the first semiconductor and being doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

3. The transistor structure of claim 2, wherein the first semiconductor is silicon.

4. The transistor structure of claim 3, wherein the second semiconductor is carbon and the first and second semiconductor form a silicon carbide crystal structure.

5. The transistor structure of claim 4, wherein the first conductivity free carriers are electrons and the second conductivity free carriers are holes.

6. The transistor structure of claim 5, wherein the first impurity is arsenic.

7. The transistor structure of claim 6, wherein the second impurity is boron.

8. A silicon on insulator transistor structure comprising:

a) an insulating oxide layer separating a device layer of semiconductor material from a bulk semiconductor base region;

b) a generally rectangular central channel region within the device layer, the central channel region consisting of a first semiconductor material doped with a first impurity element to increase first conductivity free carriers;

c) a source region and a drain region on opposing sides of the generally rectangular central channel region, both the source region and the drain region consisting of the first semiconductor material heavily doped with the first impurity element;

d) a gate adjacent the channel region and extending along a side of the central channel region adjacent the source region and forming a junction with the channel region, the gate comprising the first semiconductor material and a second semiconductor with an energy gap greater than the first semiconductor material and being doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

9. The silicon on insulator transistor structure of claim 8, further including a backgate adjacent the channel region, and on an opposing side of the channel region from the gate, and forming a junction with the channel region, the backgate comprising

the first semiconductor material and a second semiconductor with an energy gap greater than the device layer semiconductor and being doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

10. The silicon on insulator transistor structure of claim 9, wherein the first semiconductor material is silicon.

11. The silicon on insulator transistor structure of claim 10, wherein the second semiconductor is carbon and the first and second semiconductor form a silicon carbide crystal structure.

12. The silicon on insulator transistor structure of claim 11, wherein the first conductivity free carriers are electrons and the second conductivity free carriers are holes.

13. The silicon on insulator transistor structure of claim 12, wherein the first impurity is arsenic.

14. The silicon on insulator transistor structure of claim 13, wherein the second impurity is boron.

22. The transistor structure of claim 1, wherein the gate extends the entire length of the channel region between the source region and the drain region.

23. The transistor structure of claims 22, further including a backgate adjacent the channel region, extending the entire length of the channel region between the source region and the drain region, on an opposing side of the channel region from the gate,

and forming a junction with the channel region, the backgate comprising the first semiconductor and a second semiconductor with an energy gap greater than the first semiconductor and being doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

24. The transistor structure of claim 23, further including a conductive via electrically coupling the gate to the backgate.

25. The silicon on insulator structure of claim 8, wherein the gate extends the entire length of the channel region between the source region and the drain region.

26. The silicon on insulator structure of claim 25, further including a backgate adjacent the channel region, extending the entire length of the channel region between the source region and the drain region, on an opposing side of the channel region from the gate, and forming a junction with the channel region, the backgate comprising the first semiconductor material and a second semiconductor with an energy gap greater than the first semiconductor material and being doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

27. The silicon on insulator structure of claim 26, further including a conductive via electrically coupling the gate to the backgate.